

Summary of FE-I Workshop in LBL

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Originally, scheduled as 3 day FE-H Integration Workshop, then redefined as first discussion of FE-I:

- Abder Mekkaoui invited from FNAL the first day for extended discussion of BTeV experience with HP to IBM/TSMC conversion and specific pixel issues.
- Laurent Blanquart, Peter Fischer, Emanuele Mandelli, Roberto Marchesini, Gerrit Meddeler, and KFE in attendance from ATLAS pixels.

Topics and Goals:

- Discuss special concerns for using 0.25 μ processes - remaining risks ?
- Discuss current FE-H and FE-D designs, and evaluate block by block what changes are necessary or desirable. First agreements on who will do what...
- Discuss technology issues (TSMC vs IBM rules, metal layers, linear caps, etc.)
- Discuss design methods (top-down design, synthesis, CAD tools) and upgrades to design kit (back-annotated Verilog, SEU-tolerant cells, substrate contacts, etc.)
- Do we prototype in TSMC/IBM MPW first or go directly to engineering run ?

Technology Issues for Design Conversion

Power Supplies:

- Supply voltage for thin oxide is 2.7V (2.5V + 8%) maximum limited by hot carrier effects and gate oxide integrity. For thick oxide, it is 3.6V (3.3V + 8%). The equivalent number for DMILL is 5.5V.
- For burn-in purposes, the corresponding limits are 3.90V (3.75V + 4%) and 5.2V (5V + 4%) at a maximum temperature of 140C (very limited time duration). Accelerated stress testing at wafer level (“wafer screening”) is a significant component of the recommended burn-in strategy.
- Snapback voltage for thin oxide FETs is about 4.0V worst case (minimum L_{eff} , maximum temperature), and 6.0V for thick oxide. These voltages are almost 8V in DMILL, so the transient tolerance was greater.
- Thin oxide is 5nm, thick oxide is 7nm (similar to 0.35 μ process). The thick oxide will be less rad-hard, but have not seen detailed characterization. Even with thick oxide, cannot reach 4V of present opto-electronics (driven by VCSEL bias requirements after irradiation of about 2.7V).

Transistor Geometry:

- For annular NMOS layout, it is impossible to achieve $W/L < 2.3$. This affects circuits trying to reduce g_m (e.g. preamp feedback and threshold control in pixel front-end used in FE-D).

Lifetime Issues:

- We want to consider lifetimes of 10 years (= 100K hours), which is fairly standard. A high reliability chip in modern CMOS technology can achieve lifetimes of 10 FIT (= 1 failure per 10^9 hours), which would lead to about 30 FE die failures in ATLAS, so our requirements are pushing the state of the art (ignoring radiation effects), and we must pay great attention to reliability.
- Major factors for devices are hot carriers (large lateral fields in small devices inject electrons into oxide and cause threshold shifts, can be reduced by increasing L_{eff}), and gate oxide integrity (oxide lifetime is expressed in terms of Q_{bd} , charge to breakdown, which is extremely steep function of oxide field).
- Major factor in interconnects is electromigration, just as in 0.8μ , but it must be examined more carefully given small geometries and higher power densities.

Yield Issues:

- Use “R” rules to improve yield.
- Use redundant vias.
- Use recommended decoupling capacitor (a fusible 160fF MOS capacitor), and distribute uniformly to avoid altering matching of thin oxides across die.
- Design for “wafer screening”: design for static operation at EVS voltage, design for dynamic operation at DVS voltage (details forthcoming...)

Layout Rules:

- **Fill requirements:** CMP requirements limited fill factor on all interconnect layers. For metal layers, it is between 30% and 70%. There are also limits on poly and active. Note this implies that two layers are required to fully shield digital circuitry. One must also pay careful attention to crosstalk between layers which can be induced by fill patterns.
- **Antenna rules:** Due to dry plasma etch steps in modern processing, danger of large conductors connected to small area floating gates. This can cause significant threshold shifts, if not actual oxide failure. For poly case, antenna ratio should be less than 100, for metal case, less than 200. Minimize (or clamp) antennas on devices which should be matched.

ESD Rules:

- More difficult to protect properly in smaller feature size process, and devices are more delicate, so extra care required.
- Need supply-supply and ground-ground protection ? Vendor says yes.
- Potential issues with leakage in large diodes after large radiation doses ?

Summary of Issues

Access to submissions:

- IBM MPW organized by CERN as 3-metal submissions with “fixed” dates. First one relevant for us is tentatively end of Feb. 2001. Turnaround is 10-13 weeks.
- TSMC MPW organized through MOSIS in US. Relevant dates for us are Jan 2 2001, and Feb 26 2001. Turnaround is 8-10 weeks, and cost for 25 small die is \$1550/mm², or about 15-20K\$ for Analog Test Chip (about 2x4mm).
- IBM engineering run, nominally 2-6 wafers, but 12 are possible. Cost for 12 wafer run is approximately 150K\$. Scheduled when we want, and turnaround time is 10-13 weeks. Penalty of 30K\$ if total CERN engineering runs exceed 4 per year.

Comparison of TSMC and IBM:

- Processes are very similar. Production process would likely be IBM (6 metal), but TSMC (5 metal) provides second vendor and fast-turn MPW on frequent schedule.
- FNAL experience is that layout differences are minor (e.g. via sizes are 0.28μ vs 0.30μ) and SPICE differences are minor (and models are accurate), even for analog design. Common design and common design environment are possible.
- Modifications to standard cell layout needed (but also for other reasons).

- Believe the best approach for us is to start from work of CERN/RAL/FNAL to develop common IBM/TSMC environment for ATLAS pixels, but must understand legal issues. Use “R” rules from IBM, design for yield and reliability.

Goals of FE-I submission:

- Necessity of extensive testbeam and irradiation tests implies creating chip on the fastest possible schedule. H8 schedule in 2001 extends through the end of October with 2 weeks of 25ns running. An engineering run by June 1 2001 is the latest date to provide wafers and assemblies for these critical evaluation periods.
- Critical path for electronics is to build modules for assembly into “fixed” portions of system, where a “first production wafers” date of about July 1 2002 is vital.
- These are very aggressive schedules...
- A “conservative” design (equivalent to FE-H) is the best match to these goals, and using $50\mu \times 400\mu$ pixels and 32 EOC buffers is adequate. To maximize chip lifetime and reliability, propose to use 2.0V supplies for VDD and VDDA. Will start from FE-H pinout, and possibly update for power supply connections.

Issues for FE-I Control Logic:

- SEU tolerance or management is a major issue. FE-D approach was to compute parity check for critical Global configuration bits, and flag errors in EOE word.

- For FE-I, propose to build Global Register out of 8-bit blocks with Hamming code protection (all single bit errors are corrected, all double bit errors are detected). This requires 5 extra bits plus combinatorial logic, but seems possible in 0.25μ .
- Will also try to carefully analyze all logic blocks, particularly state machines, for impact of SEU. Need to eliminate “non-transient” effects that would affect more than isolated single pixels. Don’t plan for modifications in pixel control logic.

Issues for FE-I Front-end:

- Significant changes needed to replace present long NMOS required for feedback in preamp and for threshold control in discriminator (impossible to achieve W/L less than about 3 with single annular NMOS).
- This leads towards active leakage compensation, which is more flexible and robust, but has higher noise. Optimum design needs careful analysis.
- Want to control threshold with 8-bit current DACs instead of 5-bit voltage DACs (has poor dispersion for module), but keep scheme with 3-bit TDAC inside pixel.
- The major performance issue is timewalk. Possible that a two-stage design could provide better performance, with large feedback capacitor in first stage, small AC coupling capacitor, and moderate gain in second stage.
- Differential design (varying degrees exist) could provide better immunity to pickup effects, and provide more robust operation of modules and overall system.

- Another improvement would add 2-3 bits of IF tuning (feedback current, controlling TOT response) to improve quality of charge/timing measurements.
- Not clear whether we need VCCA, and whether there is still a need for the dual power pads located at 1/4 and 3/4 points of chip frame.
- Do we need some ESD protection on bump pad (plasma cleaning and sensor punchthrough are transient sources) ?

Issues for FE-I Analog Blocks:

- The present internal chopper calibration system has acceptable performance for all lab measurements except timewalk. The dual range 8-bit system has poor risetime on high range due to tradeoffs in power and RC time constants (5mA across 200Ω resistor for 60Ke full scale, and across 20Ω for 6Ke full scale). Will consider low impedance buffering of chopper, or possibly placing simple chopper in pixel cell, but significant improvements may not be possible.

Issues for FE-I Digital Readout:

- In going from FE-D to FE-H, already made significant changes in design approach, to top-down, synthesizable Verilog descriptions and more synchronous logic. Additional space in FE-I (cells in IBM are about 2.5 times smaller than cells in HSOI), allows this approach to be continued to other blocks (pixel hit logic, CEU, EOC), which will reduce the time to complete these blocks, and should lead to a more synchronous and reliable design.

- Want to make all blocks fully static, including present dynamic hit storage. This has significant design implications in column pair. First concepts discussed, but further study needed to define final approach.
- In general, 0.25 μ brings possibility of improving analog performance using additional digital circuitry. One promising idea is to perform a digital timewalk correction in the CEU. This requires moving the TOT calculation from the serializer to the CEU, and then modifying the LE timing of hits as they enter the EOC buffers, and possibly duplicating hits for ambiguous TOT values.
- Agreed to increase the number of TSI bits from 7 to 8, to remove the present tight constraint of a maximum L1 latency of 128 crossings.
- Extensive discussion of supplies and grounding. Proposal is to bring out separate connection for digital substrate (isolated from digital ground), and to consider trading present two identical VDD bond pads for two separate supplies (VDD for pixels and VDD for bottom of chip) to keep digital supplies in active area of chip as quiet as possible.

Issues for FE-I Floorplanning:

- Propose to use lower 3 metals for routing, and top 2-3 metal layers for power supplies and shielding. Note shielding is more difficult since layer fill factors must be between 30% and 70%. This also matches present 3-metal standard cells.

- May change from the FE-D/FE-H floorplan, to a more integrated analog floorplan. There appears to be more freedom, and hence less need for iteration, and advanced constraining of block aspect ratios, etc. so this is less critical.
- There will most likely be revisions to the proposed FE-H pinout, but the critical issue remains making optimal use of the central 30 bondable pads. The 20 non-power pins would probably remain unchanged (but might move their locations), and the 10 power pins might be revised.

Summary of Who does What

Bonn (Peter, Giacomo, Ivan):

- Responsibility to update cell layout for library to include TSMC compatibility, separate substrate connection, additional pixel-specific cells.
- Conversion of analog blocks from FE-D, including DACs, chopper, and threshold control. Design of Hamming-code correcting registers.
- Responsibility to integrate and submit Analog Test Chip like that included in FE-D submissions. This would be a MPW run with TSMC, targeted for Jan 02, 2001.

CPPM (Laurent, Isabelle, Moshine):

- Responsibility to develop and lay out new analog front end design. Will be on a fast track for TSMC submission, and is presently the critical path.
- Responsibility for design of biasing and threshold control, current reference, analog buffer, and LVDS I/O (if we choose to update the existing standard cells).

LBL (Emanuele, Roberto, Gerrit, Kevin):

- Overall responsibility for design environment and common TSMC/IBM rules.
- Responsibility for updated column pair readout (pixel hit logic, pixel memories, CEU, and sense amps) plus pixel control block, updated EOC buffer design, and integration into complete column pair.

- Responsibility for all digital logic at bottom of chip, which will be almost entirely synthesized and mainly placed and routed with automatic tools.
- Responsibility for overall integration of all blocks into final submission to IBM.